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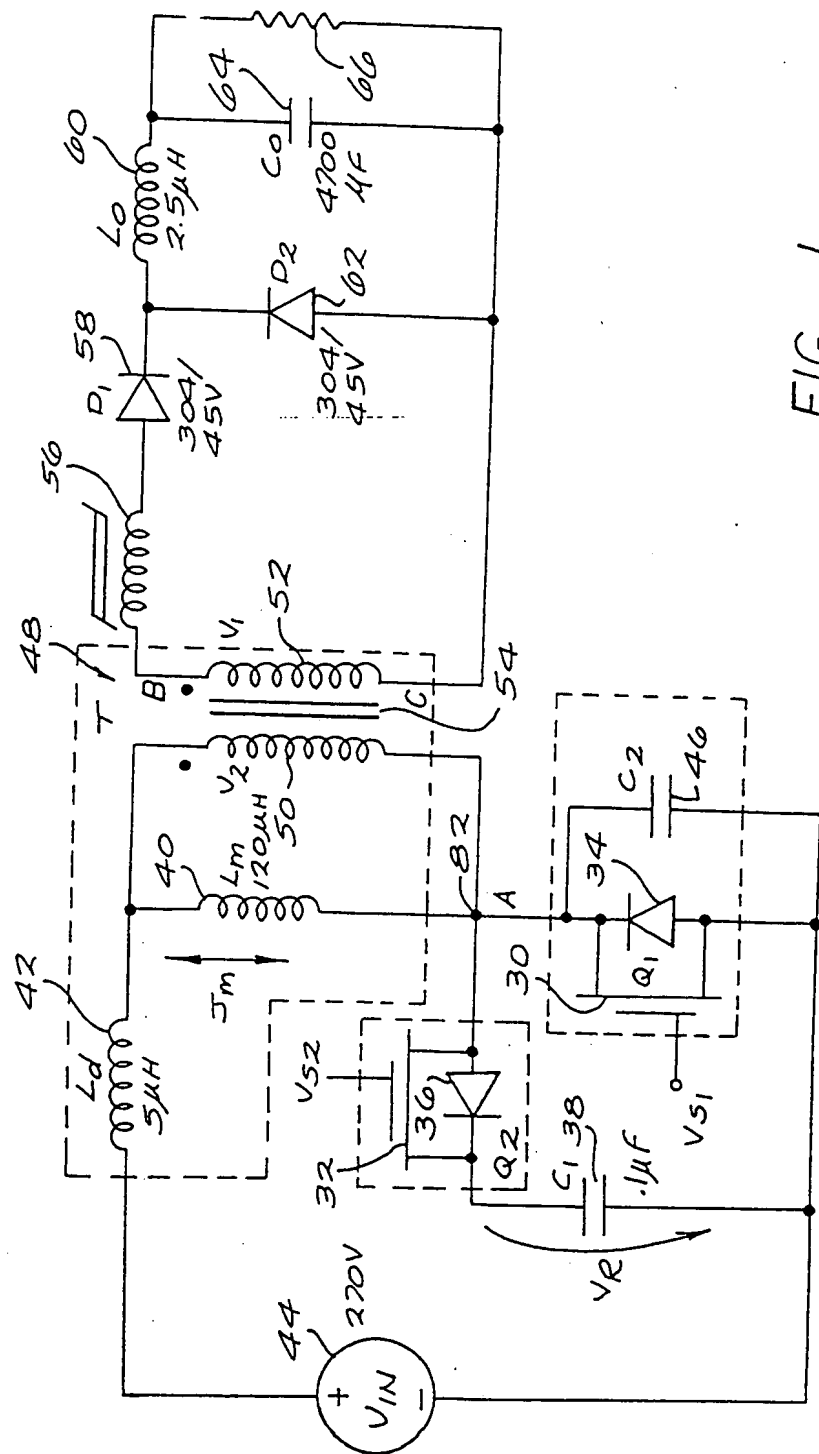
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(54) Fixed frequency single ended forward converter switching at zero voltage.

(57) A single ended forward DC-to-DC converter is operated with a main switch in series circuit with a primary winding of the isolation transformer and an auxiliary switch for charging a reset capacitor also in circuit with said primary winding. The main switch and auxiliary switch are operated through control logic so that neither switch is On at the same time. A predetermined dead time is provided between turning OFF the auxiliary switch and turning ON the main switch to allow the output capacitance of the main switch to discharge into the secondary of the transformer. Current discharge into the secondary of the transformer during this time period is limited either by a saturable reactor in series circuit with the secondary or a selectively controlled rectifier.

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This invention relates to DC-to-DC converters, and relates more specifically to forward single ended converters which switch at zero voltage and to methods of operating such converters.

A DC-to-DC converter is a circuit which converts a direct current voltage at one level to a direct current voltage at another level. If the circuit is based upon switching the input DC current through the primary of a transformer and then rectifying it in the secondary of the transformer, the converter is called a single ended forward converter. A single ended forward converter is gated by a single switch in series with the primary of the transformer. Energy is transferred forward from the input through the primary winding to the secondary winding of the transformer during the ON period of the switch.

One of the main design goals in such DC-to-DC converters is to increase the amount of power transferred through the converter. One prior art approach is presented by Fred O. Barthold in "Source Volt-Ampere/Load Volt-Ampere Differential Converter", U.S. Patent

Common prior art DC-to-DC converter topologies include the buck or forward converter, the buck-boost or flyback converter, and the boost converter which transfer energy from the input to the output during the ON time or OFF time of the main switch. In these circuits a dead time is created during the energy transfer which results in an increase in size of an output filter. Barthold combines the forward and flyback topologies to achieve a continuous transfer of energy from the input to the output of the converter to significantly reduce the size of the output filter.

Another prior art method for increasing the power transfer through the converter is to increase the switching frequency. This results in a reduction of the size of the isolation transformer and the output filter. However, there are upper limits to the operating frequency of prior art buck converters, for example, on account of switching losses in the semiconductor switches utilised in the converters. Switching losses occur when the main semiconductor switch in the buck converter is turned ON and OFF due to the finite switching speed or the time required for the current in the semiconductor device to start and stop flowing.

In order to overcome limitations in switching speeds, the prior art has devised a new family of resonant and quasi-resonant DC-to-DC converters. In the case of quasi-resonant converters, the prior art technique consists of shaping the current or voltage to become half sinusoidal and to perform the switching when the current or voltage reaches zero. The reactive elements which contribute to shaping the current or voltage are part of the basic circuit and are considered undesirable in classic topologies because of leakage inductance and parasitic capacitance. An example of one such circuit can be found in Vinciarelli, "Forward Converter Switching at Zero Current", U.S.

Patent 4,415,959. The technique utilised by Vinciarelli consists of adding a resonant capacitor across the flywheeling diode to create a resonant circuit in combination with the leakage inductance of the transformer. During the ON time of the main switch, a current charges the resonant capacitor. When the current reaches zero, the main switch turns OFF in the primary of the transformer. The output inductor discharges the resonant capacitor, transferring the energy to the load. This topology eliminates switching losses which allows the converter to run at a very high frequency. However, this topology exhibits several drawbacks which limit its utilisation at low and medium power levels. These drawbacks are as follows.

The peak current in such a quasi-resonant converter is significantly higher than in a conventional forward converter. The peak current becomes substantially large if a large input voltage range is required. The energy in the prior art device is transferred in stages from the input to the resonant capacitor and then from the resonant capacitor to the output. Due to the fact that the switching in the primary occurs at zero current and non-zero voltage, the energy contained in the output capacitance of the main switch is dissipated when it turns ON. Output power is varied by varying the frequency. A certain amount of energy is transferred from the input to the output at every cycle and when the power requirements are high, the repetition frequency is correspondingly high. Modulation of the frequency does not allow significant decrease of the output filter size. A large electromagnetic interference (EMI) filter is required to avoid beat frequency problems between the units, if two non-synchronised units are used together.

Another family of quasi-resonant converters which switch at zero voltage is described by F.C. Lee, "Pulse Width Modulation Technique", High Frequency Power Conversion International Proceedings (April 1987), Intertec Communications, Ventura, California. These prior art circuits operate similarly to those described above with the exception that the main switch turns ON and OFF at zero voltage. This has the advantage of eliminating the losses caused by the discharge of the capacitance of the switch at turn on and also decreases the driving current utilised in the MOSFET switch due to elimination of the Miller effect, i.e. induced increase in capacitance due to anode-to-cathode charging.

However, the voltage stress across the main switch and the frequency modulation which is required make this topology unattractive.

An additional group of quasi-resonant converters includes the multi-resonant converters such as were described at the High Frequency Power Conversion International Proceedings (May, 1988), Intertec Communications, Ventura, California. While operating similarly to other quasi-resonant topologies, a secondary resonant circuit is employed to decrease the

stress across the output rectifier and to reduce frequency swings over various input-output conditions of operation.

What is needed is a converter which can operate a constant frequency yet eliminates current or voltage stresses which are characteristic of prior art quasi-resonant converters while at the same time shaping the voltage or current only at the switching time.

The invention utilises a topology which uses energy accumulated in the magnetic field of the isolation transformer to discharge the output capacitance of the main switch to zero. In contrast, in the prior art technologies the magnetising energy within the isolation transformer was either recycled back to the input source or in some cases dissipated in a snubber resistor. The discharge of the capacitance of the main switch to zero prior to TURN ON of the main switch has several advantages. For example, losses caused by energy stored in the output capacitance of the main switch are eliminated since they are internally dissipated when the main switch is turned on. Switching noise from the Miller effect is eliminated. Current spikes generated at TURN ON of the main switch due to parasitic capacitance of the transformer is eliminated. A low time rate of change of the voltage arising from the quasi-resonant discharge of the capacitance of the main switch is reflected as a low rate of change of voltage across the secondary windings. This significantly reduces the current spike across the secondary windings of the transformer due to cross conduction between the main rectifying diode and the flywheeling diode in the output stage. A slow rate of change of the voltage allows the flywheel diode to recover from conduction. In the preferred embodiment, a saturable reactor is used in the secondary circuit of the transformer to delay the current flow and cross conduction between the flywheel diode and the main diode is further reduced.

The power transfer to the output is modulated by varying the duty cycle, as is commonly used in constant frequency converters.

The main switch is turned OFF prior to the voltage being built up across it. This is accomplished by a fast TURN OFF scheme and also by using an external capacitor connected across the main switch. Energy accumulated in the capacitor is not discharged through the main switch, but is cycled back to the input source.

The energy contained in the leakage inductance of the transformer is not dissipated but is also recycled back to the input source.

Another advantage of the topology of the invention is its ability to reset the transformer to eliminate the DC component from the flux density in the transformer. This leads to better utilisation of the core of the transformer for a single ended forward converter. One consequence of this resetting technique is the minimisation of the voltage stress on the primary switch. A

constant voltage is applied across the primary switch during the OFF time which is tailored to avoid the dead time. The duty cycle is not limited to a 50% constraint which is imposed by most prior art resetting techniques. The condition necessary to achieve zero voltage switching is also independent of the output current. In contrast, prior art, zero current crossing, resonant converters limit the output current in order to achieve a zero current crossing condition.

As a result of the invention switching losses are virtually eliminated; noise in the primary and secondary of the isolation transformer is significantly decreased; the available flux swing for the isolation transformer is maximised; the voltage across the main switch is minimised; limitations on the main switch duty cycle due to transformer core saturation are avoided; constraints on the output current due to zero voltage conditions are avoided; the ability to provide multiple outputs is provided; the circuit is adaptable to primary current mode control; the circuit is operable at very high frequencies without switching losses or noise; the circuit is capable of high power density conversion due to full utilisation of the transformer core, high frequency operation and constant frequency operation thereby minimising the size of the output filter; and the circuit does not require special components typical of resonant capacitors with very low equivalent series resistance.

According to one aspect of the present invention a single ended, zero-voltage switching, forward DC-to-DC converter is characterised by a DC voltage source and a transformer having a primary and secondary winding. A main switch selectively couples the voltage source across the primary winding of the transformer. An auxiliary switch selectively allows the voltage across the primary winding to reach zero. The main switch and auxiliary switch each have an OFF period and ON period. The auxiliary switch is non-conductive prior to the ON period of the primary switch by a predetermined time period sufficient to allow the voltage across the primary switch circuit to reach zero voltage. The auxiliary switch remains non-conductive until the main switch cycles through its corresponding ON period and OFF period. A reset capacitor is coupled between the auxiliary switch and AC ground of the converter. A third switch is coupled in series with the secondary winding of the transformer and selectively remains at least partially non-conductive as the voltage across the primary switch reaches decreases. The third switch becomes conductive when the voltage across the primary switch reaches zero. A first rectifier is coupled in series with the third switch for conducting current from the third switch. A control circuit selectively operates the main switch, the auxiliary switch and third switch to transfer energy through the converter by modification of the duty cycle of operation of at least the main and auxiliary switch to achieve turn ON of the primary switch at zero voltage.

The converter further comprises a discrete, resonant capacitor in parallel with the primary switch.

In an alternative embodiment converter further comprising an inductor coupled in parallel across the primary winding of the transformer in series with the auxiliary switch and the reset capacitor.

In one embodiment first rectifier and the third switch comprise a unidirectionally controlled switch circuit. The unidirectional controlled switch circuit is selectively operated by the control circuit so that it is non-conductive after the voltage across the primary switch reaches zero, and so that it is conductive during the corresponding ON time of the primary switch.

In another embodiment the transformer comprises a plurality of secondary windings.

In the preferred embodiment the third switch is a saturable reactor.

The converter further comprises a load and load inductor. The load inductor is coupled in series circuit between the first rectifier, third switch and load.

The converter further comprises a second rectifier coupled between ground of the secondary winding of the transformer and the input to the load inductor at its coupling to the first rectifier.

The control circuit comprises a sensory circuit for sensing voltage across the load. The control circuit maintains a constant voltage across the load by varying the ON period of the primary switch, the third switch or both.

The third switch is a saturable inductor or a synchronised rectifier.

The converter further comprises a voltage reference. The control circuit compares the difference in voltage across the load and the voltage reference. The difference is compared to a signal which is proportional to the current through the primary switch.

In one embodiment the converter further comprises a second transformer having a corresponding primary winding and secondary winding. The third switch comprises the secondary winding of the secondary transformer, and the control circuit applies a variable voltage to the primary winding of the secondary transformer.

According to a further aspect of the present invention, a single ended forward converter is provided in which energy is transferred from a primary winding to a secondary winding of a transformer during an ON period of a primary switch. Circuitry is provided for recycling the magnetising energy stored in the transformer to reset it during the OFF period of the primary switch such that discharge of output capacitance of the primary switch to zero is achieved prior to turn ON of the primary switch on a subsequent cycle. The invention comprises a reset capacitor. An auxiliary switch including an antiparallel diode is coupled in series with the reset capacitor. A switch control circuit operates the auxiliary switch including the antiparallel diode in accordance with a control logic such that:

(a) the auxiliary switch including the anti-parallel diode is opened prior to the ON period of the primary switch for a period of time sufficient to discharge the output capacitance of the primary switch;

(b) the auxiliary switch including the anti-parallel diode closes at the same time the primary switch opens; and

(c) the auxiliary switch including the anti-parallel diode is open during the ON period of the primary switch.

In the illustrated embodiment the auxiliary switch may comprise a field effect transistor in parallel with a discrete and/or body diode.

The converter further comprises a circuit for inhibiting current in the secondary winding of the transformer until the output capacitance of the primary switch is discharged.

According to yet another aspect of the present invention, a method of operating a single ended forward DC-to-DC converter is provided characterised by the steps of storing energy in a primary winding of a transformer by flowing DC current through the primary winding in series circuit with a primary switch. The primary switch is then turned OFF. A secondary switch in series circuit with the primary of the transformer is turned on to charge a reset capacitor. The secondary switch is turned on after the primary switch turns off. After the charge on the reset capacitor is increased to a predetermined level, the secondary switch is turned off. The current flow through the primary winding reverses and allows the output capacitance of the primary switch to discharge into the input source. The voltage across the primary switch is thus drawn down to zero, thereby allowing the primary switch to then turn on at zero voltage. Voltage discharge across the primary switch is implemented in part and facilitated by selective opening of a third switch in series with the secondary winding of the transformer.

By way of example the present invention will now be described with reference to the accompanying drawings in which:

Figure 1 is a schematic circuit diagram of a forward converter utilising the resetting methodology of the invention;

Figure 2 is a timing diagram of the circuit of Figure 1;

Figure 3a is a schematic circuit diagram wherein the current mirror resetting technique of the prior art is illustrated;

Figure 3b is a schematic circuit diagram wherein another prior art technique is illustrated;

Figure 4 is a timing diagram of the circuit of Figure 3a;

Figure 5 is a schematic circuit diagram of an output stage of a converter employing a saturable reactor according to the invention;

Figure 6 is a timing diagram of the converter output stage of Figure 5;

Figure 7 is a schematic circuit diagram of a converter employing a current mode control according to the invention;

Figure 8 is a timing diagram of the circuit of Figure 7;

Figure 9 is a simplified block schematic diagram illustrating control circuitry for use in combination with the circuit of Figure 7;

Figure 10 is a timing diagram of the control circuitry of Figure 9;

Figure 11 is a schematic diagram of another embodiment of the invention wherein a plurality of secondary windings are included in the transformer, each with its own third switch and control circuit; and,

Figure 12 is a schematic diagram of an embodiment of the invention similar to Figure 11, wherein the saturable inductor used as a third switch is replaced with a synchronised switch.

A single ended forward DC-to-DC converter is operated with a primary switch connected in series with a primary winding of an isolation transformer and an auxiliary switch for charging a reset capacitor also in circuit with the primary winding. The primary switch and the auxiliary switch are operated through control logic so that neither switch is ON at the same time. A predetermined dead time is provided between turning OFF the auxiliary switch and turning ON the primary switch to allow the output capacitance of the primary switch to discharge into the input source. Current discharge into the secondary of the transformer during this time period is limited by a third switch, which may either be a saturable reactor in series circuit with the secondary, or a selectively controlled switch.

The resetting scheme methodology utilised in connection with the forward converter of the invention can best be understood by first considering prior art resetting methodologies, such as described by Vinciarelli, "Optimal Resetting of the Transformer Core in Single Ended Forwarded Converters", U.S. Patent 4,441,146 (1984). Figures 3 and 4 of the accompanying drawings illustrate this prior art current mirror methodology. An A.C. equivalent topology is shown in Figure 3b taken from Barn, "Full-Fluxed, Single-Ended DC Converter", US Patent 4,809,148 (1989) wherein the series combination of the capacitor and auxiliary switch are coupled to the negative rail rather than the positive rail as shown in Figure 3a taken from Vinciarelli, "Optimal Resetting of the Transformer Core in Single Ended Forwarded Converters", U.S. Patent 4,441,146 (1984). For the sake of discussion ideal switches 10 and 12 are assumed in the schematic of Figure 3a. Leakage inductance, winding capacitance and other parasitic elements reflected from transformer 18 are ignored. At time T1 in Figure 4 switch 12, S2, shown in Figure 3a symbolically as a

mechanical switch, but which in practice always assumes the form of a semiconductor switch, is open. Primary switch 10, S1, is closed starting with the first ON period 20 in Figure 4. The DC voltage V_{in} is impressed upon the primary winding 16 of transformer 18 causing a magnetic flux to be propagated across the core 22 of the transformer. If N is the number of primary turns, the total change in flux is $V_{in}(T_2-T_1)/N$. The change in magnetising current is then given by $V_{in}(T_2-T_1)/L_m$ where L_m is the magnetising inductance of transformer 18.

At time T2 in Figure 4, switch 10, S1, turns OFF and switch 12, S2, turns ON. Current then flows into capacitor 24. The energy stored in the magnetising inductance of transformer 18 is then transferred into capacitor 24. After several cycles, the voltage across capacitor 24 reaches a level V_r which is a function of the input voltage, V_{in} , and the duty cycle of switch 12, S2.

In the example, the resonant frequency defined by capacitor 24 and the magnetising inductance L_m is assumed to be much lower than the repetition frequency at which switches 12 and 10 are opened and closed. As a result, the voltage across capacitor 24 does not change during the OFF period 26 of switch 10, S1, as shown in Figure 4 or conversely the ON time of switch 12, S2. Between time T2 and T3, the magnetising current is defined by $(V_r - V_{in})(T_3 - T_2)/L_m$. If the magnetising current between T2 and T3 is set equal to the magnetising current between T1 and T2, then $(V_r - V_{in})(T_3 - T_2) = V_{in}(T_2 - T_1)$. If the duty cycle of the switches 10 and 12 are then defined as equal to $(T_2 - T_1)/(T_3 - T_1)$, then V_r equals $V_{in}/(1-D)$.

The output voltage, V_0 , of the forward converter of Figure 3a is defined as $V_0 = DV_{in}/NR$, where NR is the turns ratio of transformer 18. If the output voltage is to be regulated over the range of variation of the input voltage then the duty cycle has to vary inversely with the input voltage. In other words, the duty cycle is larger at a lower input voltage and smaller at a high input voltage.

From the expression for V_r (i.e. the resetting voltage across capacitor 24) it can be concluded that the voltage across the storage capacitor 24 does not vary over a large range provided the input voltage does not vary widely.

It can be appreciated now by viewing Figure 3a that the energy of magnetisation in transformer 18 is recycled between the input source and capacitor 24; that the variable flux swing is maximised; that the voltage stress across switch 10 is minimised to the range of the variations of the input voltage; and that there are no constraints on the duty cycle.

However, according to the following description, what is avoided by the invention is the cycling of the energy of magnetisation between the input source and storage capacitor through a resistive path which is formed by the resistance of switch 12 and primary

16. This resistive path causes part of the energy to be dissipated.

Further as will be shown below, according to the invention the magnetising energy of transformer 18 is used to discharge the output capacitance of switch 10 instead of cycling it back and forth between the input source and capacitor 24.

Furthermore, the timing for switches 10 and 12 is very critical within the circuit of Figure 3a. Particular problems arise if switch 12 does not turn OFF prior to the turn ON of switch 10. Cross-conduction between switches 10 and 12 leads to very high current spikes limited only by the conductive resistance of switches 10 and 12. Avoidance of cross conduction in a forward converter with a capacitive reset switch has long been known and the use of out-of-phase switches in the primary loop for this purpose is shown by Polikarpov et. al., "Single-Cycle Direct Voltage Regulator", Soviet Patent SU 892-614 (1981). As will be described below, according to the present invention, a predetermined delay T is used to steer the magnetising current in order to discharge the output capacitance of the FET.

During transient variations of the duty cycle, the voltage across capacitor 24 changes. This change requires several cycles to complete and during that period, flux density in the core of transformer 18 could reach catastrophic values. As described below, the invention avoids this possibility by using current mode control. Peak magnetising current, which is a significant portion of the primary current in transformer 18, is kept under a predetermined level which is below saturation of the core.

The methodology of the prior art does not achieve zero voltage switching of main switch 10. This results in increased stress on switch 10 and higher power losses in the converter. Avoiding cross conduction between the main and auxiliary switches as claimed by Vinciarelli '146 and others does not achieve the advantages of zero voltage switching as practised in the invention.

Turning now to Figure 1 which illustrates the methodology of the invention it will be seen that ideal switches 10 and 12 of Figure 3a are replaced by MOSFET devices 30 and 32 which are the preferred choice because of the existence within such devices of body diodes 34 and 36, respectively, to provide a reverse current flow through the switch without an additional external diode. In Figure 1 the circuit equivalent of the actual MOSFET devices has been illustrated within a dotted outline. The body diodes 36 and 34 thus represent the parasitic diode within the actual MOSFET. Similarly the circuit equivalent of transformer 48 is illustrated within a corresponding dotted outline and includes the parasitic magnetisation inductance L_m and the load inductance L_d . The design of the circuit is thus made by taking into account the parasitic or actual characteristics of practical devices used in it.

Control signals VS1 and VS2 are provided to the gates of MOSFETs 32 and 34 from a control circuit, the timing of which is described below in connection with Figure 2 and which is itself described later in greater detail in connection with Figures 7 and 9. MOSFETs 32 and 34 are controlled so that there is a predetermined time interval, T, between the turn OFF of switch 32 and the turn ON of main or primary switch 30. At the moment when reset switch 32 turns OFF, the current flowing through it flows from storage capacitor 38 through the magnetising inductance 40, L_m , and input load inductance 42, L_d , toward the input voltage source 44, V_{in} . The magnetising current tries to continue its flow by flowing through capacitor 46, magnetising inductance 40 and load inductance 42 toward the input voltage source 44. The excess energy stored within the magnetic field in transformer 48 causes body diode 34 to conduct and allows zero voltage switching to occur in switch 30. The timing delay between the switching cycles of switches 30 and 32, as shown by T in timing lines 68 and 74 of Figure 2, is solely determined by the discharge path characteristics from switch 30 through the inductance of transformer 48 to input source 44. This in turn is affected by a third switch 56 described below.

Consider the following simplified analysis of Figure 1. Assume, for example, that the drain-to-source output capacitance of each switch 30 and 32 is constant. This is actually true only if a supplementary capacitor is added in parallel with the switch, because, generally, the drain-to-source capacitance of a MOSFET is dependent upon the voltage across the MOSFET. Secondly, assume that the ON state resistance of each MOSFET switch 30 and 32 and DC resistance of primary winding 50 of transformer 48 is negligible. The current through a saturable reactor 56 is negligible for a period of time when the voltage across switch 30 decreases to zero.

In order for switch 30 to turn on at zero voltage the following equation has to be satisfied:

$$I_m^2 L_m > C V_r^2 \text{ where } V_r = V_{in}/(1-D),$$

where I_m is the magnetisation current flowing through transformer 48.

During the ON state of main switch 30, the magnetising current varies by amount dI and $I_m = dI/2$. The corresponding increment in the current flowing through the magnetisation inductance L_m is DTV_{in}/L_m where D is the duty cycle and T is a repetition period. The magnetising current, I_m , then is one half this value. Returning to the inequality above and substituting the expressions for the resetting voltage V_r and magnetising current I_m results in the inequality:

$$1/(2 L_m C^{1/2}) > F_r / D(1-D)$$

where F_r is the repetition frequency. The left side of the inequality is the resonant frequency of the magnetising current and the output capacitance of switch 30, which will be re-designated as a single quantity ω_r .

the resonant frequency. The inequality can then be restated as:

$$f D(1-D) > Fr. \quad (1)$$

The quantity $D(1-D)$ has a maximum value at $D=0.50$. Therefore, main switch 30 will turn ON at zero voltage provided that repetition frequency is less than a certain factor of the resonant frequency. Consider now the delay time introduced by saturable reactor 56. It is well known that the product of the peak voltage and delay time of an inductive reactor is a constant. Therefore the higher the input voltage the smaller the delay time. Also, for a regulated output as described above, the higher the input voltage the smaller the duty cycle. The most critical condition for zero voltage switching is therefore experienced at high input voltage.

From the above relationship it can immediately be concluded that zero voltage switching occurs independently of the magnitude of the output current. The resonant frequency, f , of the circuit should be selected to satisfy the inequality (1) specified above over all input and output conditions. Since the output capacitance of switch 30 is a fixed factor due to the MOSFET structure, only the magnetising inductance can be varied to set the resonant frequency.

Transformer 48 comprises a primary coil 50 and secondary coil 52 with a magnetising core 54. Secondary coil 52 is in series circuit with a saturable inductor 56 and main diode 58. The output of the circuit is provided to a load inductance 60, a load resistance 66 and load capacitance 64, the latter two of which are in parallel with each other. A flywheel diode 62 is also coupled across the output.

The operation of the circuit of Figure 1 is illustrated in the timing diagram of Figure 2. Graph line 68 corresponds to the gate voltage applied to main switch 30 illustrating ON state periods 70 and OFF state periods 72. Graph line 74 similarly corresponds to the gate voltage applied to secondary switch 32. OFF periods 76 are alternated with ON state periods 78. However, as can be seen by comparing graph lines 68 and 74, a time gap T or "dead" time is provided between T_1 and T_2 following an ON state 78 of secondary switch 32 and before ON state 70 of main switch 30. As previously discussed T is determined by the discharge time of switch 30.

Similarly there is a "dead" time between times T_3 and T_4 following ON state 70 of main switch 30 and before ON state 78 of secondary switch 32 during which neither of switches 30, 32 is conducting. The delay T_4-T_3 can be arbitrarily provided so that $0 < T_4-T_3 < (1-D)/2Fr$. Graph line 80 corresponds to the voltage at node 82 which represents the voltage across main switch 30. Again by comparison of graph lines 80 and 68 it can be appreciated that the ON state 70 of main switch 30 occurs only when the voltage across the main switch 30 is zero.

Graph line 84 represents the current through

main switch 30. The current through saturable inductor 56 is represented on graph line 86 as will be described in greater detail below. The voltage differential across the secondary 52 of transformer 48 is depicted by graph line 88. The timing relationships of the input and output voltages and currents in the primary and secondary windings of transformer 48 are illustrated by graph lines 80-88 of Figure 2. As seen by comparing graph lines 80 and 84, positive current flows in switch 30 only after the voltage across switch 30 reaches zero. As seen from graph line 88, the slope of the rising edge of the voltage across the secondary winding is decreased in proportion to the slope of the falling edge of the voltage across switch 30 as seen from graph line 80, so that ringing in the secondary is significantly decreased.

One feature of the topology of the invention is the time delay introduced by saturable inductor 56. Figure 6 is a timing diagram which shows the relationship of several signals and the output of the circuit of Figure 1 as shown in Figure 5. Graph line 81 represents the voltage across main switch 30. The voltage across both saturable inductor 56 and secondary 52 is represented by the graph line 90 in Figure 6. The current through the saturable inductor, I_L , and the current flowing through flywheel diode 62 are shown on graph line 92.

At time T_1 auxiliary switch 32 turns OFF as shown in Figure 2 and the magnetising current starts to flow from the output capacitance of main switch 30, here primarily due to the capacitance of capacitor 46. This current is represented by graph line 84 in Figure 2. The voltage across main switch 30 is shown in enlarged time scale on graph line 81 of Figure 6. At the moment the voltage across main switch 30 becomes equal to the input voltage, V_{in} , indicated at time T_2 in Figure 6, the voltage reflected in secondary coil 52 reaches zero as depicted on graph line 88 of Figure 2. The voltage across secondary coil 52 thereafter is in the process of becoming positive.

If saturable inductor 56 were not present, main diode 58 would be forward biased and the current would flow into the secondary circuit, thereby transferring part of the energy contained in the magnetic field created by the magnetising current to the secondary of the circuit. If this were to occur, it would not allow enough magnetising energy to be returned to the input source to discharge the output capacitance of main switch 30 and thus obtain zero voltage switching. To prevent this, saturable inductor 56, LS , is included in series circuit within the secondary output.

For low level currents through saturable inductor 56, inductor 56 exhibits high inductance. Once the current flowing through it reaches a predetermined level, inductor 56 saturates and effectively becomes an electrical short circuit. The time delay introduced by saturable inductor 56 is chosen to be larger than the time difference T_3-T_2 in Figure 6, which is the time

interval during which the voltage across main switch 30 decreases from V_{in} to zero.

Graph line 92 shows that little current flows through saturable inductor 56 until T_3 is approached. The exponential shape of the current of the saturable reactor as shown by graph line 92 is typical of its saturable characteristic. Graph line 90 is representative of the voltage between the anodes of main diode 58 and flywheel diode 62. Main diode 58 is back biased until at least time T_2 and until current begins to flow through saturable inductor 56 at about time T_3 . The voltage then applied to the anode of main diode 58 is the input voltage multiplied by the turns ratio of transformer 48.

Thus it can be appreciated from Figure 6 by comparing graph lines 81 and 92 that the time delay introduced by saturable inductor 56 between T_2 and T_3 allows for the full discharge of the output capacitance of main switch 30 and the transfer of that discharge energy through transformer 48 into the output circuit.

It must be understood that it is entirely consistent with the present invention that the time delay exhibited by saturable inductor 56 could be replaced by a synchronised switch which turns on after the voltage of main switch 30 reaches zero.

One of the drawbacks of prior art forward converters is that at the time the main switch turns OFF, the voltage rises sharply in the secondary creating current spikes which flow through the main diode and flywheel diode. To prevent this problem dissipating snubbing circuitry is required in the prior art. However, in the circuit described above, the voltage across main switch 30 decreases in a quasi-resonant fashion and at the same time the voltage reflected into the secondary exhibits a similar quasi-resonant behaviour. This soft waveform in the secondary allows flywheel diode 62 to turn OFF less abruptly prior to the build up of the current through main diode 58. This operation significantly decreases the power dissipation in diode 62 and decreases the noise level.

In the context of the above description, main or primary switch 30 and auxiliary switch 32 are gated by external control signals which are derived through conventional control circuitry. However, a control circuit according to the invention is described in connection with Figures 7 and 8. Turning to the schematic circuit diagram of Figure 7, the circuit of Figure 1 is shown as controlled through a current mode control.

Because a significant portion of the primary current comprises magnetising current, an inner feedback loop controls the flux density in main transformer 48 by controlling the peak current. This eliminates the risk of saturation of the transformer core during transients which are associated with this resetting technique. The lack of current ringing at turn ON of main switch 30 at zero voltage and the presence of a gentle slope of the magnetising current as shown on graph line 84 of Figure 2 makes current mode control imple-

mentation more effective and easier.

Turning now to Figure 7, wherein main switch 30 is shown as resistively coupled to ground through resistor 94 for current mode control, the gate of main switch 30 is driven by latch 96 which is set by a clock 98. Latch 96 is reset by the output of a comparator 100. The inputs to comparator 100 are the voltage between the series combination of main switch 30 and resistor 94 on one hand, and the output of an error amplifier 102 on the other. Error amplifier 102 is a differential amplifier operating between a reference voltage and the output voltage coupled from the secondary circuit, namely the output load inductance 60.

The output of latch 96 is also used as a trigger signal for reset logic circuit 104. The gate of secondary transistor 32 is driven by reset logic circuit 104. Secondary or auxiliary switch 32 is in parallel with an anti-parallel diode 106. Anti-parallel diode 106 includes both internal and external diodes to transistor 32. An anti-parallel diode is defined for the purposes of this specification as a diode coupled in parallel with a switch, wherein the direction of current flow through the diode is opposite to the normal direction of current flow through the switch.

Figure 8 is the timing diagram of the circuit of Figure 7. Graph line 108 illustrates the clock pulses generated by clock circuit 98 provided as the set signal to latch 96. The output of latch 96 is depicted on graph line 110. The voltage sensed from resistor 94 is indicated by pulses 112 on graph line 114. The output of error amplifier 102 is a constant voltage level, V_{error} , depending upon the difference, if any, between the reference voltage and the output voltage. When V_{error} and the voltage at resistor 94 at the output of main switch 30 is equal, comparator 100 generates a trigger pulse which resets latch 96 as shown on graph line 110. The latch output is set by clock circuit 98. The latch output shown on graph line 110 is used to drive the gate of main switch 30. The same output is provided to reset logic circuit 104 for driving auxiliary switch 32 according to the teachings of the invention. The gate drive of auxiliary switch 32 will be complemented and delayed in a manner similar to that described in connection with Figure 2 using conventional timing and logic techniques.

Turning now to Figure 9 which shows a simplified block diagram for generating timing signals of the invention, this has a corresponding timing diagram shown in Figure 10. The current mode control output from latch 96 is shown by graph line 114 in Figure 10 and is provided at output 116 of latch 96 in Figure 9. The time period between latch output pulses 118 is T . Pulse 118 is coupled in common to a rise time delay, generally denoted by reference numeral 120, and a fall time delay 122. The voltage at node 124 is depicted by graph line 126 in Figure 10 while the voltage at node 128 is depicted by graph line 130. The filtered

pulses shown on graph line 120 are then input into inverter and driver 132 whose output is depicted on graph line 134 of Figure 10. These pulses are provided to auxiliary switch 32 and are delayed by time ΔT_1 after the fall of the voltage at 124.

The pulses depicted on graph line 130 may then be input into a conventional controlled delay circuit 136. The amount of delay introduced by delay circuit 136 into the pulse can be varied according to a signal which is representative of the voltage across main switch 30. The output of controlled delay circuit 136 is then coupled through a buffer 138 and is depicted on graph line 140. The delay ΔT_2 is controlled according to the voltage across main switch 30 and is provided to ensure that there is a gap or dead time between the gating signal provided to switches 30 and 32 to ensure the operation of the device as previously described in connection with Figures 2 and 6. It must be clearly understood that many other types of controllers can be utilised for timing in addition to those illustratively set forth here.

Another embodiment of the invention similar to that described in Figure 7 is schematically illustrated in Figure 11 where a plurality of secondary coils 52(1)-52(m) are included within transformer 48, each with a corresponding secondary output circuit. Each of the secondary circuits in Figure 11 has its own third switch 56(1)-56(m), which is shown in each case as a saturable inductor. The first secondary circuit corresponding to coil 52(1) is provided with the feedback control described in Figure 7 through control circuit 140. Each of the other secondary circuits corresponding to coils 52(2)-52(m) have separate corresponding control circuits 140(2)-140(m) in the secondary circuit to individually set each output circuit.

Still another embodiment of the invention is depicted in Figure 12 which shows a circuit similar to that shown in Figure 11 but in which the saturable inductor of the secondary circuit corresponding to coil 52(1) has been removed and a synchronised switch 142 has been substituted in lieu thereof. Switch 142 is controlled by control circuit 144 according to the teachings of the invention to effect a zero voltage switching, which control circuit also provides the feedback control from the secondary output circuit to the primary output circuit as shown in Figures 7 and 11.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. For example, instead of using current mode control, voltage mode control, or multiple loop feedback control can be substituted.

Moreover, any kind of switch now known or later devised may be used, including N or P type FET power devices which may be substituted for the main and auxiliary switches, the carrier type of the main and auxiliary switches may be interchanged with each other, and the reset capacitor may be connected to

the positive source or return.

Claims

1. A single ended, zero-voltage switching, forward DC-to-DC converter, characterised by a DC voltage source (44), a transformer (48) having a primary (50) and secondary (52) winding and main switching means for selectively coupling the voltage source across the primary winding of the transformer and further characterised by auxiliary switching means (32) for selectively allowing the voltage across the primary winding (50) to reach zero, the main switching means (30) and auxiliary switching means (32) each having an OFF period and an ON period with the auxiliary switching means being non-conductive prior to the ON period of the main switching means by a predetermined time period sufficient to allow the voltage across the main switching means to reach zero voltage and with the auxiliary switching means remaining non-conductive until the main switching means cycles through its corresponding ON period and OFF period, by a reset capacitor (38) coupled between the auxiliary switching means and AC ground of the converter, by third switching means (56, 142) coupled in series with the secondary winding (52) of the transformer (48) for selectively remaining at least partially non-conductive as the voltage across the main switching means decreases, the third switching means becoming conductive when the voltage across the main switching means reaches zero, by a first rectifier means (58) coupled in series with the third switching means for conducting current from the third switching means and by a control circuit means (140, 144) for selectively operating the main switching means, auxiliary switching means and third switching means to transfer energy through the converter by modification of the duty cycle of operation of at least the main and auxiliary switching means to achieve turn ON of the main switching means at zero voltage.
2. A converter according to claim 1, further characterised by a discrete, resonant capacitor (46) connected in parallel with the main switching means.
3. A converter according to claim 1, characterised in that the first rectifying means and the third switching means comprises a unidirectionally controlled switch means (142) selectively operated by the control means (144) so that the unidirectionally controlled switching means is non-conductive after the voltage across the main switching means reaches zero and is conductive during corresponding ON time of the main switching means.

4. A converter according to claim 1, characterised in that the transformer (48) comprises a plurality of secondary windings (52(1) to 52(m)).
5. A converter according to claim 1, characterised in that third switching means is a saturable reactor (56).
6. A converter according to claim 1, characterised by a load (66) and a load inductor (60) which is coupled in series circuit between the first rectifying means (58) and the load (66).
7. A converter according to claim 6, characterised in that a second rectifying means (62) is coupled between ground of the secondary winding (52) of the transformer (48) and the input to the load inductor (60) at its coupling to the first rectifying means (58).
8. A converter according to claim 6, characterised in that the control circuit means (140) comprises sensory means for sensing voltage across the load and maintains a constant voltage across the load by varying the ON period of the main switching means (30).
9. A converter according to claim 6, characterised in that the control circuit means (144) comprises sensory means for sensing voltage across the load and maintains a constant voltage across the load by varying the ON period of the third switching means (142).
10. A converter according to claim 6, characterised in that the control circuit means (144) comprises sensory means for sensing voltage across the load and maintains a constant voltage across the load by varying the ON period of both the main switching means (30) and the third switching means (142).
11. A converter according to claim 6, characterised in that the third switching means is a saturable reactor (56).
12. A converter according to claim 6, characterised in that the third switching means is a synchronised switch (142).
13. A converter according to claim 6, characterised by a voltage reference (REF) and by sensory means (102) for sensing voltage across the load and for comparing the difference in voltage across the load and the voltage reference, the difference being compared to a signal proportional to the current through the main switching means (30).
14. A single ended forward converter in which energy is transferred from a primary winding to a secondary winding of a transformer during an ON period of a primary switch, and in which circuitry is provided for recycling the magnetising energy stored in said transformer to reset it during the OFF period of said main switch such that discharge of output capacitance of said main switch to zero is achieved prior to turn ON of main switch on a subsequent cycle, the converter being characterised by a reset capacitor (38), an auxiliary switch (32) including an anti-parallel diode (106) coupled in series with the reset capacitor (38), switch control means operating the auxiliary switch including the anti-parallel diode in accordance with a control logic such that:
 - (a) the auxiliary switch (32) including the anti-parallel diode (106) is opened prior to the ON period of the main switch (30) for a period of time sufficient to discharge the output capacitance of the main switch (30),
 - (b) the auxiliary switch (32) including the anti-parallel diode (106) closes at the same time the main switch (30) opens, and
 - (c) the auxiliary switch (32) including the anti-parallel diode (106) is open during the ON period of the main switch (30).
15. A converter according to claim 14, further characterised by means for inhibiting current in the secondary winding of the transformer until the output capacitance of the main switch is dissipated.
16. A converter according to claim 15, characterised in that the means is a saturable reactor (56) in series circuit with the secondary winding (52) of the transformer.
17. A method of operating a single ended forward DC-to-DC converter characterised by the steps of storing energy in a primary winding (50) of a transformer (48) by flowing DC current through the primary winding in series circuit with a main switch (30), turning OFF the main switch, allowing the output capacitance of the main switch to discharge through the primary winding into a secondary winding (52) of the transformer until discharged and turning ON a secondary switch (32) in series circuit with the primary of the transformer to charge a reset capacitor (38), the secondary switch being turned ON only after there is zero voltage across the main switch.
18. A method according to claim 17, further characterised by the step of inhibiting current flow through the secondary winding (52) of the transformer until the output capacitance of the main switch is completely dissipated therethrough.

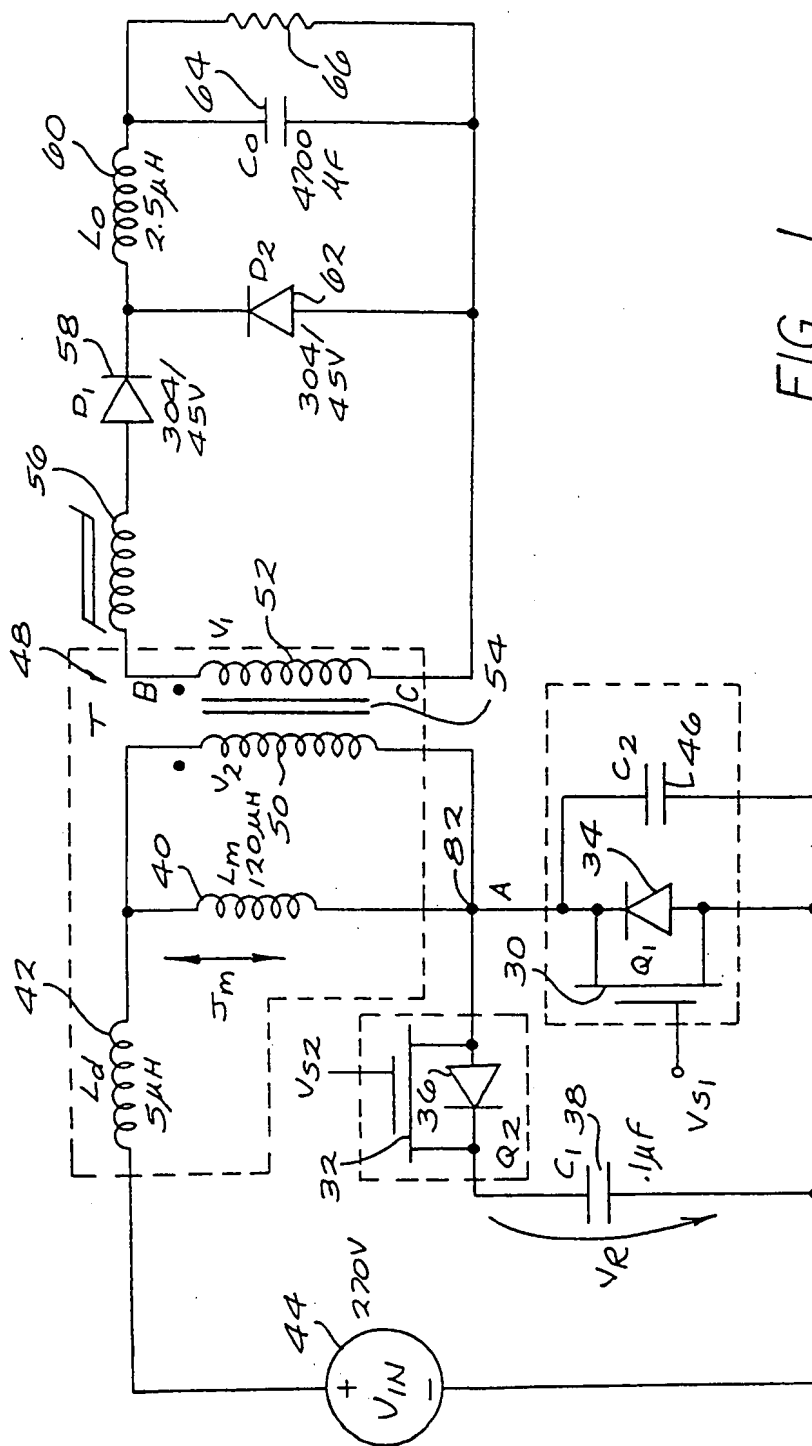


FIG. 1

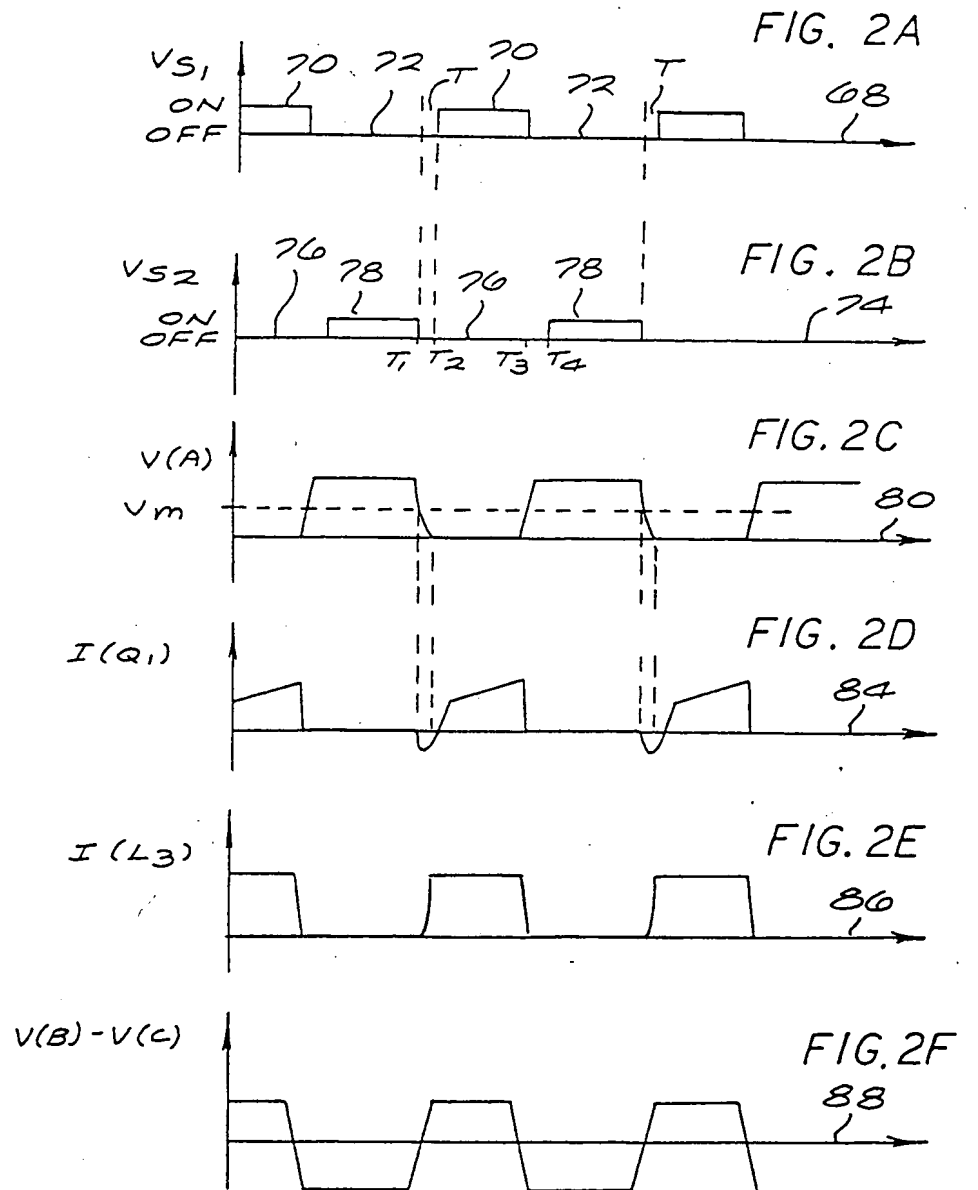


FIG. 3A PRIOR ART

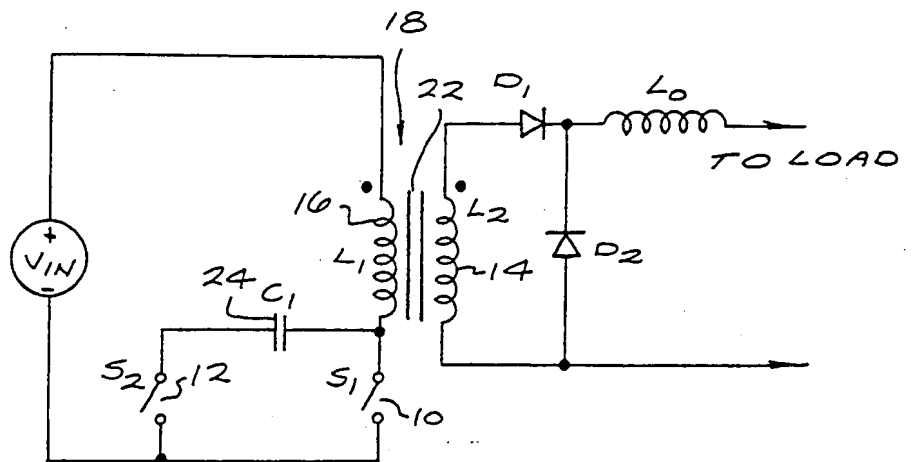
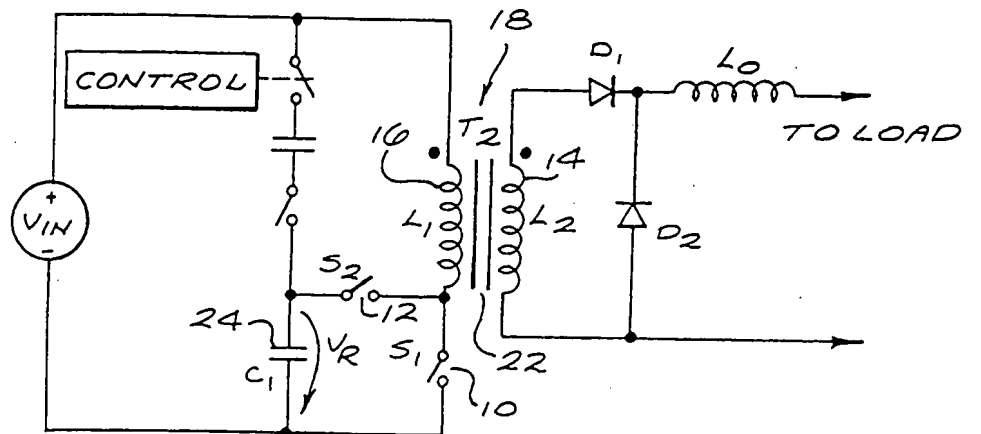


FIG. 3B PRIOR ART

FIG. 4A
PRIOR ART

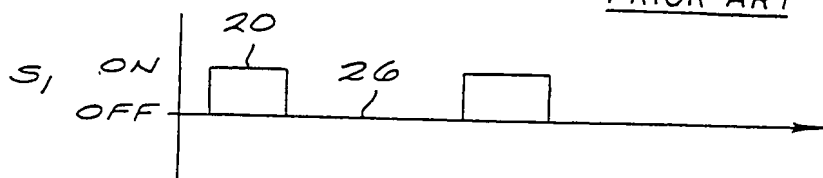


FIG. 4B
PRIOR ART

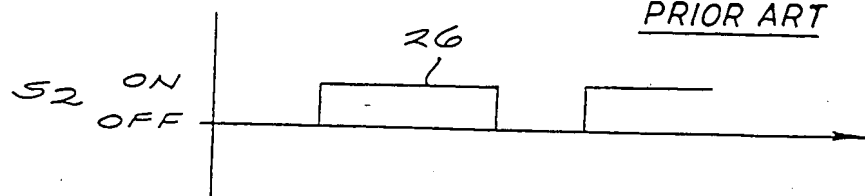


FIG. 4C
PRIOR ART

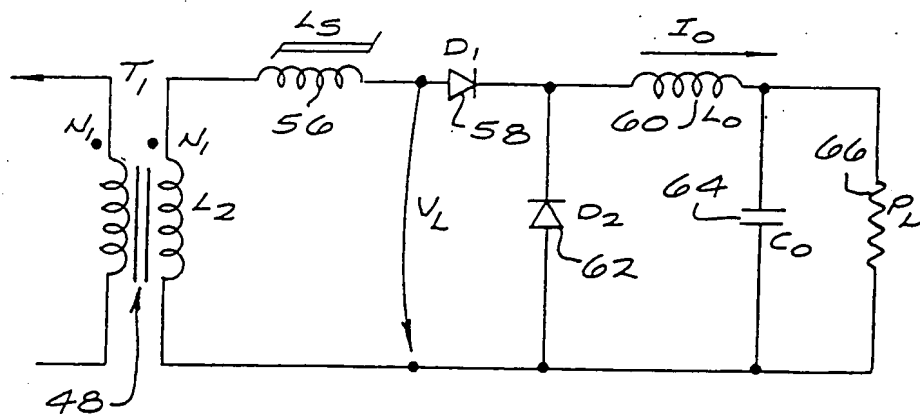
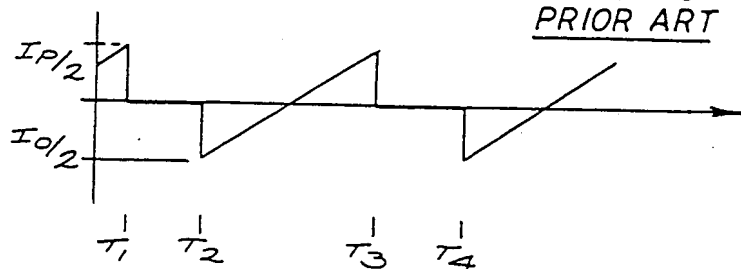


FIG. 5

FIG. 6A

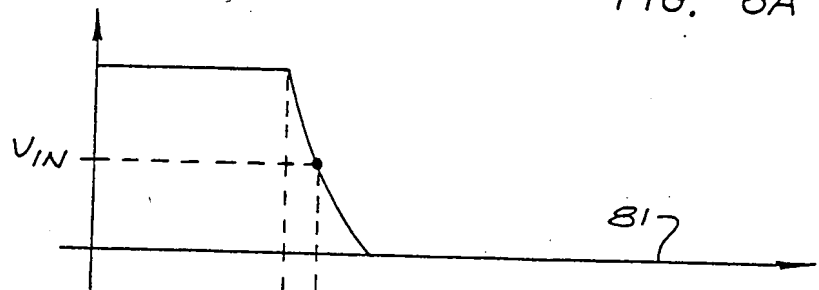


FIG. 6B

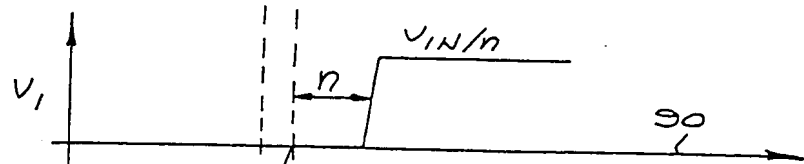


FIG. 6C

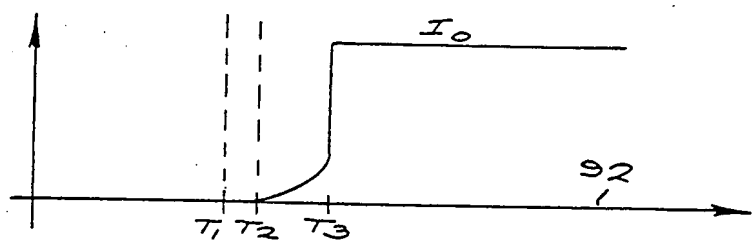


FIG. 6D

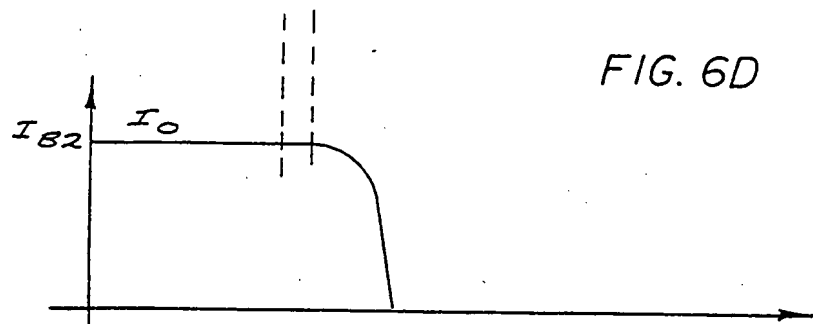
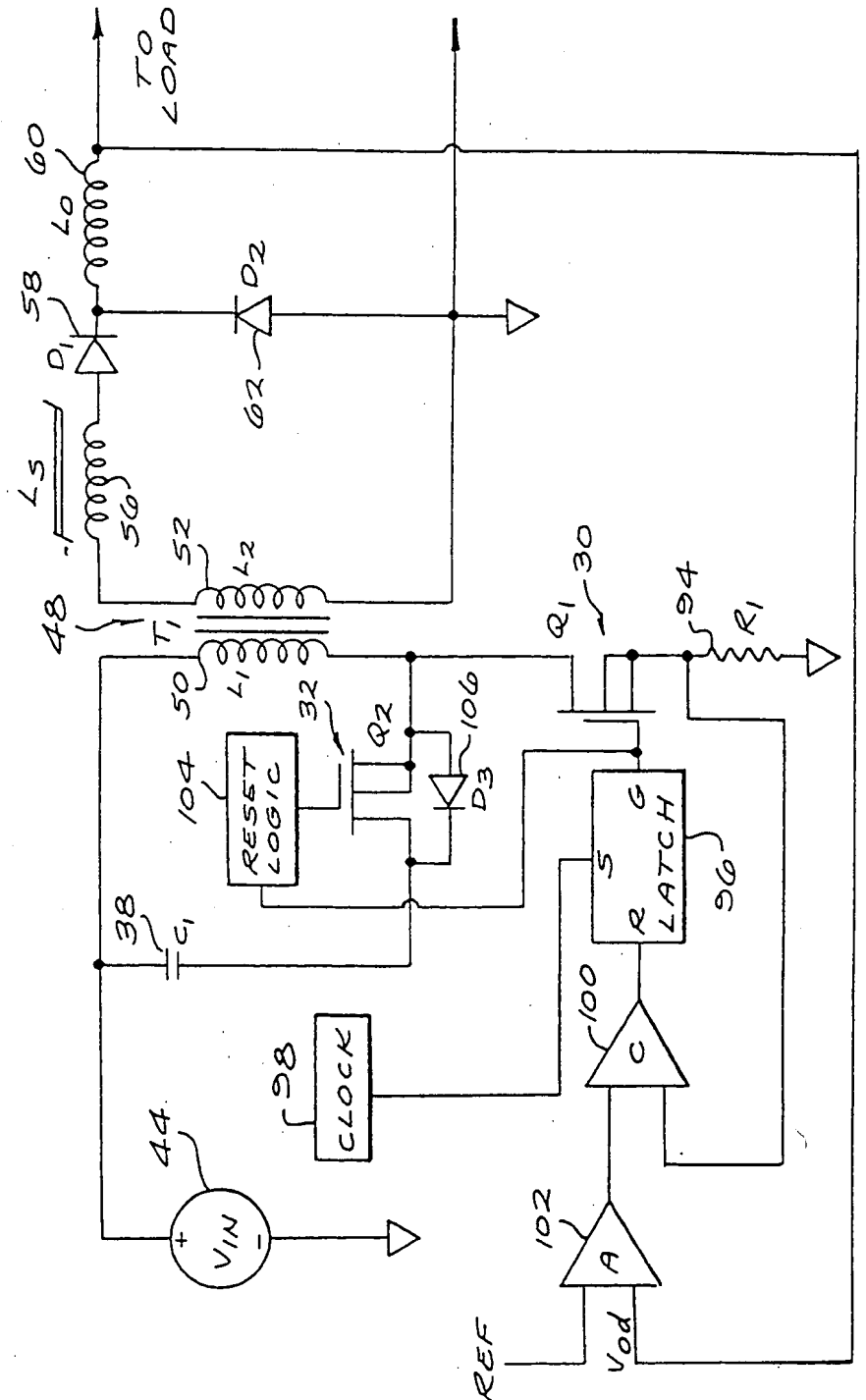
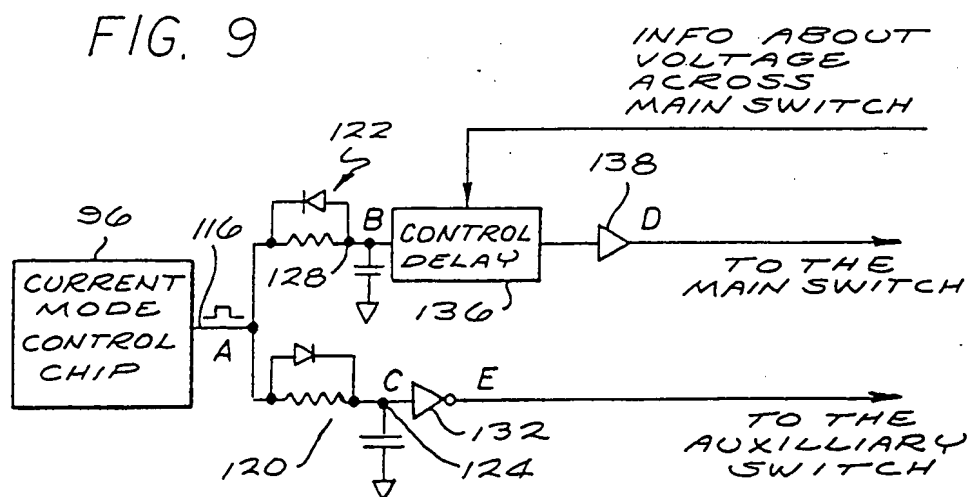
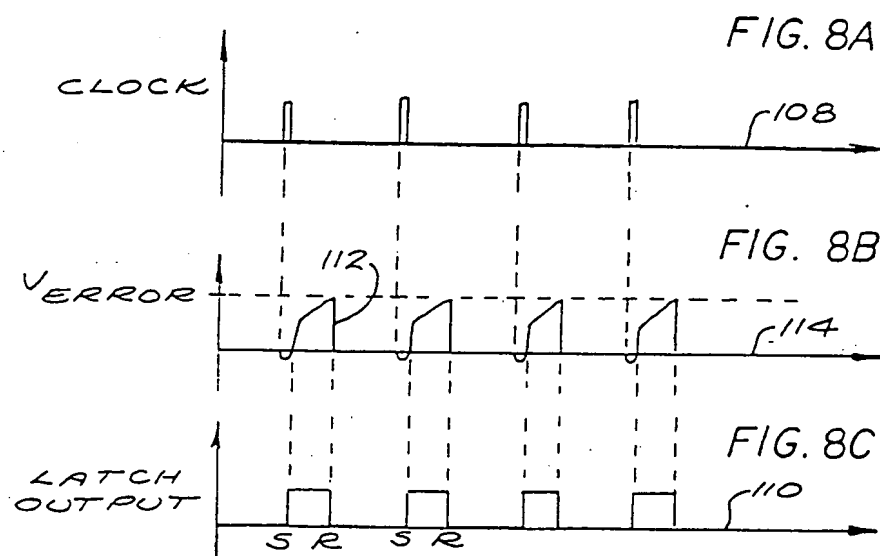


FIG. 7





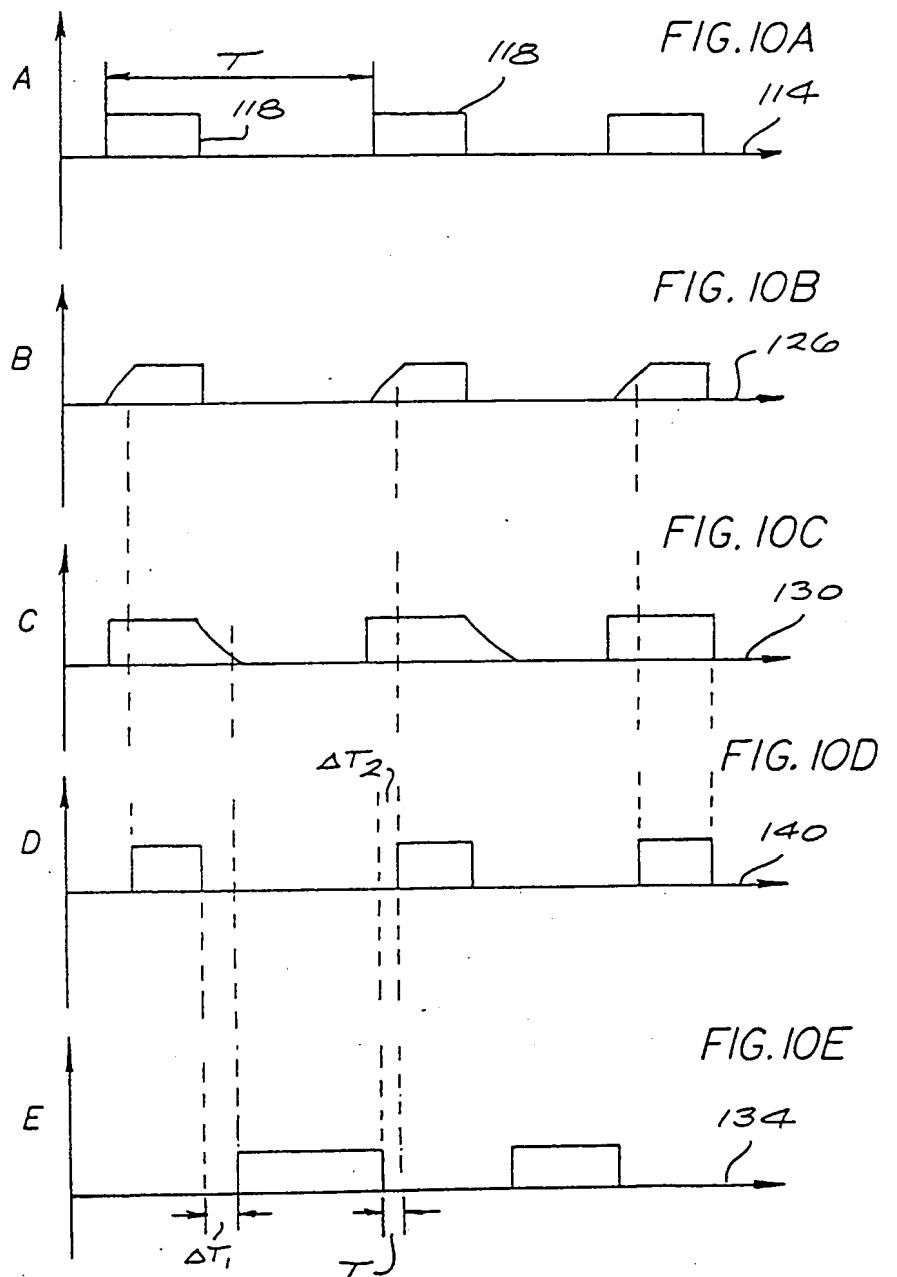


FIG. 11

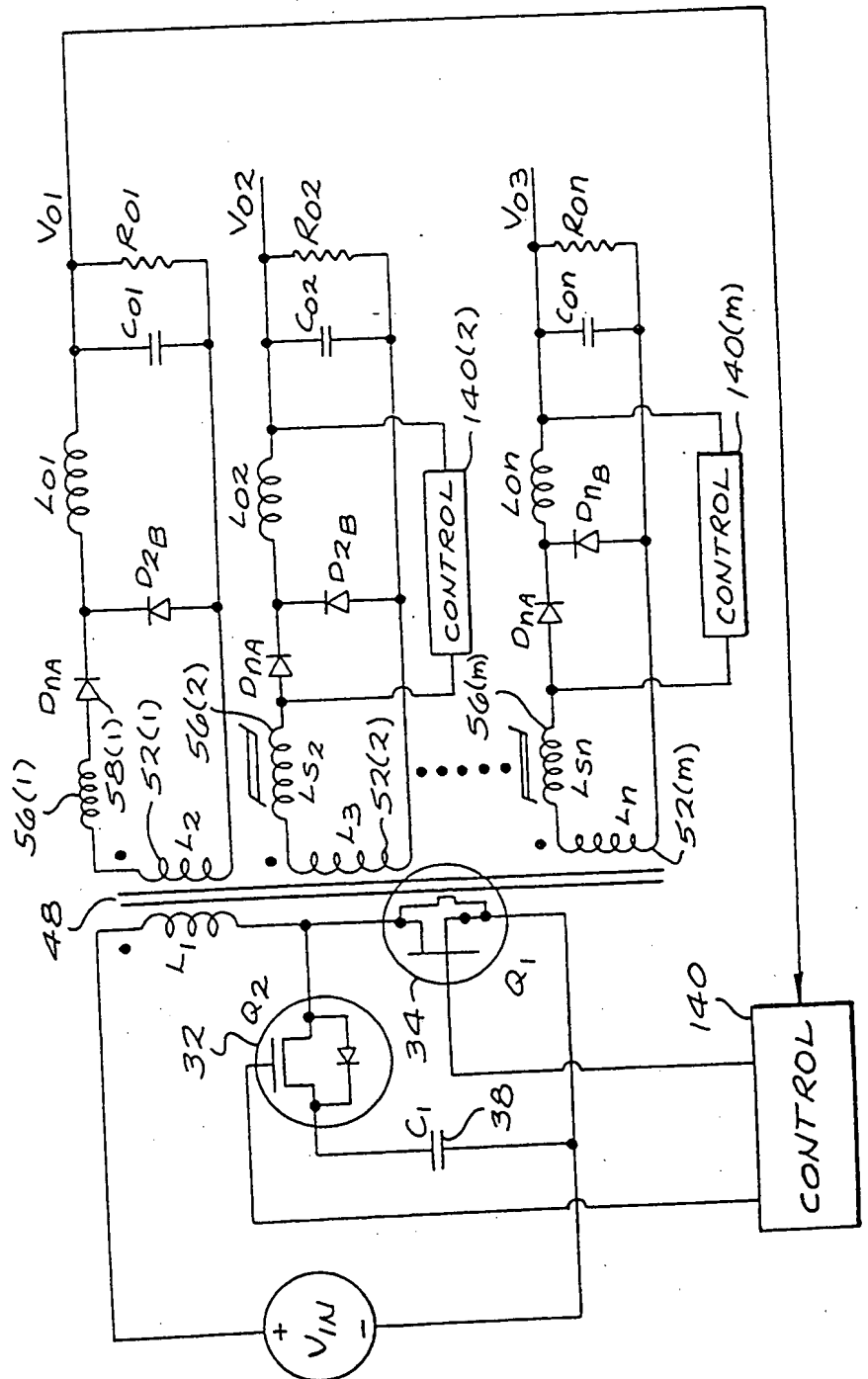


FIG. 12

